WHAT IS CLAIMED IS:

1. A test block for a memory circuit, wherein the test block is configured to characterize in situ a sensing offset of a sensing circuit including a cross-coupled pair of transistors.

2. The test block, as recited in claim 1, wherein the test block selectively introduces discharge paths into respective halves of a differential circuit sensed by the sensing circuit.

3. The test block, as recited in claim 2, wherein the discharge paths are selectively introduced to characterize a direction of the sensing offset.

4. The test block, as recited in claim 2, wherein the discharge paths are selectively introduced to characterize a magnitude of the sensing offset.

5. The integrated circuit, as recited in claim 1,
wherein the sensing offset results, at least in part, from an accumulated data-dependent mismatch in characteristics of the cross-coupled transistors.

6. The integrated circuit, as recited in claim 1,
wherein the sensing offset results, at least in part, from a disparate, negative bias temperature instability induced shift in threshold voltage (V_t) of at least one of the cross-coupled transistors based on disparate voltage bias histories thereof.

7. The integrated circuit, as recited in claim 1,
wherein the sensing offset results, at least in part, from process variations in either the transistors or differential pair circuits to which the transistors are coupled.

8. An integrated circuit comprising:
a first and a second plurality of control signals;
a first and a second plurality of ports; and

at least a first and a second discharge path coupled to at least one of the respective first and second plurality of ports, the effective strengths of the first and second discharge paths determined by respective ones of the first and second plurality of control signals.

9. The integrated circuit, as recited in claim 8, wherein the first and the second discharge paths are selectively loaded to vary the strengths of the first and the second discharge paths.

10. The integrated circuit, as recited in claim 8, wherein the first and the second discharge paths are selectively enabled, the first and the second discharge paths selected from respective ones of a first and a second plurality of discharge paths of varying strengths.

11. The integrated circuit, as recited in claim 8, wherein the first and the second plurality of control signals selectively couple at least respective ones of a first and a second capacitive load to the respective ones of the first and the second plurality of ports.

12. The integrated circuit, as recited in claim 8, wherein the first and the second plurality of control signals selectively couple at least a first and a second resistive load to the respective ones of the first and the second plurality of ports.

13. The integrated circuit, as recited in claim 8, wherein the first and the second plurality of control signals selectively enable at least one of a first plurality of transistors and at least one of a second plurality of transistors coupled to respective ones of the first and the second plurality of ports.

14. The integrated circuit, as recited in claim 8, wherein the first and the second plurality of control signals selectively enable at least one of a first plurality of inverters and at least one of a second plurality of inverters coupled to respective ones of the first and the second plurality of ports.

15. The integrated circuit, as recited in claim 8, further comprising:

a first and a second opposing bitline selectively coupled to the first and the second discharge paths.

16. The integrated circuit, as recited in claim 8, further comprising:
a control block for generating the first and second plurality of control signals based at least in part on detection of a sensing offset of a sensing circuit including a cross-coupled pair of transistors.

17. The integrated circuit, as recited in claim 16,
wherein the control block generates additional control signals, the additional control signals at least partially compensating for the detected sensing offset by selectively exposing one of the transistors to a bias voltage selected to cause a compensating shift in a characteristic of the exposed transistor.

18. The integrated circuit, as recited in claim 16,
wherein the sensing offset results, at least in part, from an accumulated data-dependent mismatch in characteristics of the cross-coupled transistors.

19. The integrated circuit, as recited in claim 16,
wherein the sensing offset results, at least in part, from a disparate, negative bias temperature instability induced shift in threshold voltage (V_t) of at least one of the cross-coupled transistors based on disparate voltage bias histories thereof.

20. The integrated circuit, as recited in claim 16,
wherein the sensing offset results, at least in part, from process variations in either the transistors or differential pair circuits to which the transistors are coupled.

21. The integrated circuit, as recited in claim 17,
wherein the transistors are PMOS devices;
wherein the characteristic is threshold voltage (V_t); and

wherein the sensing offset involves a monotonic increase in V_t based on disparate voltage bias histories of the PMOS devices.

22. The integrated circuit, as recited in claim 16, further comprising:
the sensing circuit including the cross-coupled pair of transistors.

23. The integrated circuit, as recited in claim 16, further comprising:
the differential circuit.

24. The integrated circuit, as recited in claim 8, embodied in computer readable descriptive form suitable for use in design, test, or fabrication of an integrated circuit.

25. The integrated circuit, as recited in claim 8, embodied in a cache of a processor integrated circuit.

26. A method of detecting in situ a sensing offset in a sensing circuit including a pair of cross-coupled transistors comprising:
selectively configuring a pair of discharge paths in a first configuration;
introducing the pair of discharge paths into respective halves of a differential circuit; and
sensing the differential circuit.

27. The method of claim 26, further comprising:
characterizing a direction of the sensing offset based at least in part on a value sensed in presence of the discharge paths in the first configuration.

28. The integrated circuit, as recited in claim 26,
wherein the sensing offset results, at least in part, from an accumulated data-dependent mismatch in characteristics of the cross-coupled transistors.

29. The integrated circuit, as recited in claim 26,
wherein the sensing offset results, at least in part, from a disparate, negative bias temperature instability induced shift in threshold voltage (V_t) of at

least one of the cross-coupled transistors based on disparate voltage bias histories thereof.

30. The integrated circuit, as recited in claim 26,
wherein the sensing offset results, at least in part, from process variations in either the transistors or differential pair circuits to which the transistors are coupled.

31. The integrated circuit, as recited in claim 28,
wherein the transistors are PMOS devices;
wherein the characteristic is threshold voltage (V_t); and
wherein the sensing offset involves a monotonic increase in V_t based on disparate voltage bias histories of the PMOS devices.

32. The method of claim 26, wherein the first configuration substantially balances the discharge paths.

33. The method of claim 26, further comprising:
selectively configuring the pair of discharge paths in a second configuration;
characterizing a magnitude of the sensing offset based at least in part on a value sensed in presence of the discharge paths in the second configuration.

34. The method of claim 26, wherein the second configuration imbalances the discharge paths.

35. The method of claim 34, further comprising:
successively changing the imbalance of the discharge paths by selectively reconfiguring the pair of discharge paths; and
characterizing a magnitude of the sensing offset based at least in part on a value sensed in presence of the successively changed imbalance of the discharge paths.

36. The method of claim 26, wherein the third configuration introduces to the discharge paths an imbalance incrementally varied from prior configurations.

37. The method of claim 26, wherein the characterization occurs during burn-in.

38. The method of claim 26, wherein the characterization occurs subsequent to burn-in.

39. The method of claim 26, wherein the characterization occurs periodically.

40. The method of claim 26, wherein the characterization occurs in response to sensing memory errors.

41. An apparatus comprising:

means for detecting in situ a sensing offset in a sensing circuit that includes a cross-coupled pair of transistors; and

means for characterizing a magnitude of the sensing offset.

42. The apparatus of claim 41, further comprising

means for characterizing a direction of the sensing offset.